



Staff/Sr. Staff RFIC Design Engineer

Reporting To: Chief Technology Officer

Company: IO Semiconductor, Inc.

Location: San Diego

Job Description and Responsibilities

As RFIC Design Engineer you will perform RFIC circuit design, optimization, and worst-case analysis. This includes schematic capture, simulation, layout, parasitic extraction, and design documentation AWR Analog Office tools. You must be disciplined and able to follow established design practices. As a Staff level Design Engineer you will be expected to take leadership responsibilities on design projects and to provide guidance and mentorship to junior level Design Engineers.

Required Skills and Experiences

- MSEE, or equivalent required, PHD preferred
- Minimum 8-10 years (10+ for Sr. Staff) in CMOS RFIC Design Required
- Experience as lead designer for full-custom RF CMOS wireless communication circuit designs (at transistor level) which have achieved high-volume production required
- Experience with, and in-depth knowledge of, RF layout practices and optimization of RF passive elements (i.e. inductor, varactors, etc...) required
- In-depth knowledge of parasitic extraction from IC layout, package and PCB required
- Experience with, and in-depth knowledge of, RF circuit characterization and bench testing required
- Experience with key circuit blocks, such as T/R Switch, LNA, Power Amplifier, DC:DC Converter, Charge Pump, required
- In-depth knowledge of RF device physics and device models required
- System knowledge of Cellular RF Front End architectures is required
- Proficiency with AWR Analog Office Design Tools is preferred